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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/079,666 | 02/20/2002 | Darel N. Emmot | 10001769 -1 | 7066 |

7590 06/23/2004

HEWLET-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
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EXAMINER

NGUYEN, HAU H

| ART UNIT | PAPER NUMBER |
|----------|--------------|
| 2676 | |

DATE MAILED: 06/23/2004

6

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|---------------------------------|---------------------------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/079,666 | EMMOT, DAREL N. <i>[Signature]</i> | |
| | Examiner Hau H Nguyen | Art Unit 2676 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 April 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments with regard to double patenting rejection has been fully considered, but they are not persuasive. In response to Applicant's arguments that claims 1-7 are not identical to claims 13-17 of the co-pending application 10/079,667, the examiner could not find the difference in independent claim 1 of the present application and claim 13 of the co-pending application 10/079,667. Rejection of double patenting is maintained until Applicant explains the difference between the above claims.

Claim Rejections - 35 USC § 101

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-7 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 13-20 of copending Application No. 10/079,667. This is a

provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 8-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Shino (U.S. Patent No. 6,466,219).

Referring to claims 8-9, 21-22, Shino teaches a memory configured to store pixel data in regions (2 X 8 pixels) as shown in Figs. 4-6. Shino teaches the data rearrangement unit 400 (a controller) in the "local to local" transfer mode, when reading data from one rectangular memory region in a memory region bf the DRAM 147 (Fig. 2) and transferring (writing) it to another rectangular memory region, receives as input the 256 bits of color data mc_0dtr to mc_7dtr for 8 pixels from the read controller 390, generates the color data cwr by shifting the same in accordance with origin coordinates of the rectangular memory region of the transfer destination, and outputs to the distributor 300 an address ADRW2 including the representative point coordinates (btrx, btry) (associating a reference pixel with a pixel region) used in the write operation at the destination and the valid flag btrvld (check bit) (col. 13, lines 13-25). Shino teaches the

valid flag btrvld is comprised of 16 bits and indicates whether to perform a re-write of the stored contents for every memory region of each pixel at the time of writing to the DRAM 147 in units of the rectangular memory region of 16 pixels by 8 pixels (X-direction) X 2 pixels (Y-direction). Each bit of the valid flag btr coordinate vld corresponds to a 1-pixel memory region of the 16 -pixel memory region as a unit of write operation. Each bit of the valid flag btrvld indicates a logical value "0" (check bit is set) when masking the corresponding memory region (when not performing re-write) (which implies pixel region is the same), while indicates a logical value "1" (check bit cleared) when not masking (when performing re-write) (which implies pixel region has been changed) (col. 16, lines 15-27).

In regard to claim 10, Shino further teaches the unit blocks R0 to RBA-1 are, as shown in FIG. 6, stored in the DRAM 147 comprising the texture buffer 147a so as to have continuous addresses (sequential memory addresses) in a one-dimensional address space (col. 8, lines 57-63).

In regard to claims 11 and 23, Shino teaches in the data rearrangement unit 400, representative coordinates (btrx, btry) corresponding to the above color data cwd0 to cwd4 and a valid flag btrvld are generated in an address generation unit 430 (col. 16, lines 1-4) (composing reference pixel data).

Referring to claims 12-14, Shino teaches reading from the DRAM 147 is performed in units of a rectangular memory region storing the color data of 8 pixels by 8 pixels (X-direction) X 1 pixel (Y-direction) based on the representative point (col. 14, lines 36-44). As shown in Fig. 6, block of pixel data is stored in sequential addresses, and

Fig. 14 shows how reference pixel is retrieved and how pixel data is output to display (col. 16, lines 62-67, and col. 17, lines 1-30).

In regard to claims 15-16, as cited above, with reference to Figs. 4-6, Shino teaches the predetermined pixel region (8 X 2) pixels corresponding to a predetermined region of the associated display.

Referring to claims 17-19, Shino teaches the address generation unit 430 of the data rearrangement unit 400 shown in FIG. 8 calculates, based on an address ADRR1 input from the host interface circuit 149, representative coordinates (sbx, sby) in the order of increasing X-coordinates in the scan line direction from the top left end of FIG. 19 in the X- and Y-coordinate system shown in FIG. 19. Then, an address ADRR2 including the representative coordinates (sbx, sby) is output to the distributor 300 (col. 18, lines 38-46).

In regard to claim 20, Shino teach the data length of one pixel could be 32 bits, 16 bits, 8 bits, and 4 bits (col. 12, lines 60-61). Therefore, memory location for one pixel can be 32-bit.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

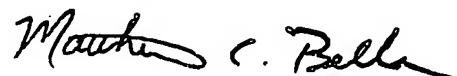
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

06/17/2004



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600